CLAIMS

What is claimed is:

1. A method of designing an integrated circuit (IC) device having desired electrical characteristics, said method comprising:

providing an initial IC device design;

generating a layout representation corresponding to the initial IC device design;

simulating how structures within the layout representation will pattern on a wafer;

based on the simulating step, determining whether actual electrical characteristics associated with the initial IC device design sufficiently match the desired electrical characteristics; and

if the actual electrical characteristics associated with the initial IC device design do not sufficiently match the desired electrical characteristics, modifying the initial IC device design.

2. The method of claim 1, wherein the step of determining whether the actual electrical characteristics associated with the initial IC device design sufficiently match the desired electrical characteristics includes:

determining actual dimensions of structures within the layout representation based on the simulating step; and

determining the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation.

3. The method of claim 2, wherein the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation are determined using a look-up table.

4. The method of claim 2, wherein the actual electrical characteristics associated with the actual dimensions of the structures within the layout

representation are determined using an electrical modeling program in which the actual dimensions of the structures are input.

5. The method of claim 1, wherein the desired electrical characteristics include at least one of drive current, gain and switching speed.

6. The method of claim 1, wherein the step of generating a layout representation corresponding to the initial IC device design includes minimizing the scale of the layout representation.

7. The method of claim 1, wherein the initial IC device design includes a desired relationship between at least two structures within the IC device design.

8. The method of claim 7, further comprising:

determining an amount of process-related variation associated with at least two structures within the layout representation of the IC device design.

9. The method of claim 8, wherein determining an amount of process-related variation associated with at least two structures within the layout representation includes:

simulating how structures within the layout representation will pattern on a wafer; and

measuring a feature of the simulated structures, said feature being indicative of process-related variation.

10. The method of claim 9, wherein the feature indicative of process-related variation is at least one of (i) slope of edge intensity and (ii) logarithm of slope of edge intensity.

11. The method of claim 10, wherein:

a larger slope of edge intensity or logarithm of slope of edge intensity is indicative of a smaller process-related variation; and

a smaller slope of edge intensity or logarithm of slope of edge intensity is indicative of a larger process-related variation.

12. The method of claim 9, said method further comprising:

measuring the feature indicative of process-related variation for one or more simulated structures over a process window of focus and intensity.

13. The method of claim 12, wherein the simulated structures are at different locations within the layout representation.

14. The method of claim 9, wherein simulating how structures within the layout representation will pattern on a wafer includes simulating how structures within the layout representation will pattern as a function of at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design, (iii) orientation of a structure, (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures.

15. The method of claim 9, further comprising:

determining whether at least a portion of the IC device design is optimized with respect to process-related variations.

16. The method of claim 15, further comprising:

if a portion of the IC device design is not optimized with respect to process-related variations, modifying at least a portion of the IC device design.

17. The method of claim 16, wherein modifying at least a portion of the IC device design includes modifying at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design, (iii) orientation of a structure, (iv) placement of a structure within a portion of the

IC device design, and (v) size of a structure with respect to other adjacent structures.

18. The method of claim 9, wherein the process-related variations include variations caused by at least one of (i) mask generation, (ii) wafer patterning, (iii) pre-patterning processing, and (iv) post-patterning processing.

19. The method of claim 11, further comprising:

providing feedback to a designer regarding how a given structure will print on a wafer as a function of at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design, (iii) orientation of a structure, (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures.

20. An integrated circuit (IC) device designed by the method of claim 1.

21. A method of designing an integrated circuit (IC) device, said method comprising:

providing an initial IC device design;

generating a layout representation corresponding to the initial IC device design; and

determining an amount of process-related variation in how at least a portion of the layout representation will pattern on a wafer.

22. The method of claim 21, further comprising:

determining whether at least a portion of the IC device design is optimized with respect to process-related variations; and

if a portion of the IC device design is not optimized with respect to process-related variations, modifying at least a portion of the IC device design.

23. The method of claim 22, wherein modifying at least a portion of the IC device design includes modifying at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design, (iii) orientation of a structure, (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures.

24. The method of claim 21, wherein determining an amount of process-related variation in how at least a portion of the layout representation will pattern on a wafer includes:

simulating how structures within the layout representation will pattern on a wafer; and

measuring a feature of the simulated structures, said feature being indicative of process-related variation.

25. The method of claim 24, wherein the feature indicative of process-related variation is at least one of (i) slope of edge intensity and (ii) logarithm of slope of edge intensity.

26. The method of claim 24, said method further comprising:

measuring the feature indicative of process-related variation for one or more simulated structures over a process window of focus and intensity.

27. The method of claim 26, wherein the simulated structures are at different locations within the layout representation.

28. The method of claim 21, further comprising:

determining whether the layout representation will pattern as an IC device having desired electrical characteristics.

29. The method of claim 28, wherein determining whether the layout representation will pattern as an IC device having desired electrical characteristics includes:

simulating how structures within the layout representation will pattern on a wafer; and

based on the simulating step, determining whether actual electrical characteristics associated with the initial IC device design sufficiently match the desired electrical characteristics.

30. The method of claim 29, wherein the step of determining whether the actual electrical characteristics associated with the initial IC device design sufficiently match the desired electrical characteristics includes:

determining actual dimensions of structures within the layout representation based on the simulating step; and

determining the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation.

31. A computer-implemented method in which an initial integrated circuit (IC) device design is provided, said method comprising:

generating a layout representation corresponding to the initial IC device design;

simulating how structures within the layout representation will pattern on a wafer;

based on the simulating step, determining an amount of process-related variation in how at least a portion of the layout representation will pattern on a wafer; and

determining whether the layout representation will pattern as an IC device having desired electrical characteristics.